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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/740,694	12/19/2000	Rick Pekkala	BAN:0104	4584

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HUFFMAN LAW GROUP, P.C.
1832 N. CASCADE AVE.
COLORADO SPRINGS, CO 80907-7449

EXAMINER	
HAN, CLEMENCE S	

ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 07/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/740,694	PEKKALA ET AL.	
	Examiner	Art Unit	
	Clemence Han	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-15,17-22,24,26,28-30,33,37,43 and 45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-15,17-22,24,26,28-30,33,37,43 and 45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 9-14, 18-22, 26, 28-30, 33, 37, 43 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bloch et al. (US Pub. 2001/0043564) in view of Iliadis (US 5,995,486).

Regarding to claim 9, Bloch teaches a method for buffering packets transmitted to an Infiniband port by an Infiniband device linked to the port, comprising: providing a portion of a memory for buffering the packets, wherein the portion has a size A (See actual spare buffer space in [0009]); transmitting flow control credits to advertise to the device buffering resources of a size B (See maximum spare allocations in [0009]), wherein B is greater than A; determining when the portion is filled with a predetermined amount of the packets [0053]; and transmitting flow control credits to the device to stop transmission of the packets in response to said determining [0053]; and providing a second memory for buffering the packets transmitted subsequent to said determining [0043], wherein said

providing a second memory comprises providing a second memory having a size C [0043]. Bloch, however, does not explicitly teach said size C is based on an amount of data that may be transmitted to the port during a latency time required to stop transmission of the packets in response to said determining. Iliadis teaches said size C is based on an amount of data that may be transmitted to the port during a latency time required to stop transmission of the packets in response to said determining (Column 4 Line 60). It would have been obvious to one skilled in the art to modify Bloch to have size C based on an amount of data that may be transmitted to the port during a latency time required to stop transmission of the packets in response to said determining as taught by Iliadis in order to avoid losses of in-transit packets (Column 2 Line 37-39).

Regarding to claim 10, Iliadis teaches said latency time comprises an approximate amount of time required to perform said transmitting flow control credits to the device to stop transmission of the packets in response to said determining (Column 4 Line 60).

Regarding to claim 11, Bloch teaches said transmitting flow control credits to the device to stop transmission of the packets in response to said determining comprises transmitting a flow control packet with zero credits for each of a plurality of virtual lanes configured on the port [0046].

Regarding to claim 12, Iliadis teaches said latency time comprises an approximate amount of time required for the port to transmit a maximum-sized Infiniband data packet to the device (Column 4 Line 54-60).

Regarding to claim 13, Iliadis teaches said latency time comprises an approximate amount of time required for the device to transmit a maximum-sized Infiniband data packet to the port (Column 4 Line 54-60).

Regarding to claim 14, Iliadis teaches said latency time comprises an approximate amount of time required for the device to respond to said transmitting flow control credits to the device to stop transmission of the packets in response to said determining (Column 5 Line 24).

Regarding to claim 18, Bloch teaches a method for buffering packets transmitted to an Infiniband port by an Infiniband device linked to the port, comprising: providing a portion of a memory for buffering the packets, wherein the portion has a size A (See actual spare buffer space in [0009]); transmitting flow control credits to advertise to the device buffering resources of a size B (See maximum spare allocations in [0009]), wherein B is greater than A; determining when the portion is filled with a predetermined amount of the packets [0053]; and transmitting flow control credits to the device to stop transmission of the packets in response to said determining [0053]; and buffering the packets transmitted by the

device subsequent to said determining in a reserved amount of the portion of the memory, wherein said reserved amount is beyond the predetermined amount [0043]. Bloch, however, does not explicitly teach said reserved amount is based on an amount of data that may be transmitted to the port during a latency time required to stop transmission of the packets in response to said determining. Iliadis teaches said reserved amount is based on an amount of data that may be transmitted to the port during a latency time required to stop transmission of the packets in response to said determining (Column 4 Line 60). It would have been obvious to one skilled in the art to modify Bloch to have the reserved amount based on an amount of data that may be transmitted to the port during a latency time required to stop transmission of the packet in response to said determining as taught by Iliadis in order to avoid losses of in-transit packets (Column 2 Line 37-39).

Regarding to claim 19, Iliadis teaches said latency time comprises an approximate amount of time required for the port to transmit a flow control packet for each of a plurality of virtual lanes configured on the port (Column 4 Line 60).

Regarding to claim 20, Iliadis teaches said latency time comprises an approximate amount of time required for the port to transmit a maximum-sized Infiniband data packet to the device (Column 4 Line 54-60).

Regarding to claim 21, Iliadis teaches said latency time comprises an approximate amount of time required for the device to transmit a maximum-sized Infiniband data packet to the port (Column 4 Line 54-60).

Regarding to claim 22, Iliadis teaches said latency time comprises an approximate amount of time required for the device to respond to said transmitting flow control credits to the device to stop transmission of the packets in response to said determining (Column 5 Line 24).

Regarding to claim 26, Bloch teaches a method for buffering packets transmitted to an Infiniband port by an Infiniband device linked to the port, comprising: providing a portion of a memory for buffering the packets, wherein the portion has a size A (See actual spare buffer space in [0009]); transmitting flow control credits to advertise to the device buffering resources of a size B (See maximum spare allocations in [0009]), wherein B is greater than A; determining when the portion is filled with a predetermined amount of the packets [0053]; and transmitting flow control credits to the device to stop transmission of the packets in response to said determining [0053]. Bloch, however, does not explicitly teach said providing a portion of a memory for buffering the packets comprises providing the memory in response to user input. Iliadis teaches said providing a portion of a memory for buffering the packets comprises providing the memory in

response to user input (Column 8 Line 66-67). It would have been obvious to one skilled in the art to modify Bloch to provide the memory in response to user input as taught by Iliadis in order to increase the throughput of the link (Column 8 Line 65-66).

Regarding to claim 28, Bloch teaches a method for buffering packets transmitted to an Infiniband port by an Infiniband device linked to the port, comprising: providing a portion of a memory for buffering the packets, wherein the portion has a size A (See actual spare buffer space in [0009]); transmitting flow control credits to advertise to the device buffering resources of a size B (See maximum spare allocations in [0009]), wherein B is greater than A; determining when the portion is filled with a predetermined amount of the packets [0053]; and transmitting flow control credits to the device to stop transmission of the packets in response to said determining [0053]. Bloch, however, does not explicitly teach advertising at least two maximum-sized Infiniband packets worth of flow control credits for each of a plurality of virtual lanes configured on the port. Iliadis teaches advertising at least two maximum-sized Infiniband packets worth of flow control credits for each of a plurality of virtual lanes configured on the port (Column 4 Line 54-60). It would have been obvious to one skilled in the art to modify Bloch to advertise at least two maximum-sized Infiniband packets worth of

flow control credits for each of a plurality of virtual lanes configured on the port as taught by Iliadis in order to avoid losses of in-transit packets (Column 2 Line 37-39).

Regarding to claim 29, Bloch teaches a method for buffering packets transmitted to an Infiniband port by an Infiniband device linked to the port, comprising: providing a portion of a memory for buffering the packets, wherein the portion has a size A (See actual spare buffer space in [0009]); transmitting flow control credits to advertise to the device buffering resources of a size B (See maximum spare allocations in [0009]), wherein B is greater than A; determining when the portion is filled with a predetermined amount of the packets [0053]; and transmitting flow control credits to the device to stop transmission of the packets in response to said determining [0053]. Bloch, however, does not explicitly teach configuring a plurality of virtual lanes on the port prior to said transmitting flow control credits to advertise to the device buffering resources of a size B. Iliadis teaches configuring a plurality of virtual lanes on the port prior to said transmitting flow control credits to advertise to the device buffering resources of a size B (Column 8 Line 51-60). It would have been obvious to one skilled in the art to modify Bloch to configure a plurality of virtual lanes on the port prior to said transmitting flow control credits to advertise to the device buffering resources of a

size B as taught by Iliadis in order to control the connections independently (Column 8 Line 49-51).

Regarding to claim 30, Iliadis teaches a product of a number of said plurality of virtual lanes and a number of bytes comprising two maximum-sized Infiniband packet exceeds size A (Column 4 Line 54-60).

Regarding to claim 33, Bloch teaches a method for controlling flow of packets into a plurality of ports on an Infiniband device, comprising: providing a memory for buffering the packets, wherein the memory has a size A (See actual spare buffer space in [0009]); transmitting flow control credits by the plurality of ports to advertise packet buffering resources of a size B (See maximum spare allocations in [0009]), wherein B is greater than A; and transmitting flow control credits by at least one of the plurality of ports to stop transmission of the packets into the at least one port in response to determining an amount of free space in the memory drops below a predetermined threshold [0053]. Bloch, however, does not explicitly teach said predetermined threshold is based on an amount of data that may be transmitted to the plurality of ports during a latency time required to stop transmission of the packets in response to said determining. Iliadis teaches said predetermined threshold is based on an amount of data that may be transmitted to the plurality of ports during a latency time required to stop transmission of the

packets in response to said determining (Column 4 Line 60). It would have been obvious to one skilled in the art to modify Bloch to have said predetermined threshold is based on an amount of data that may be transmitted to the plurality of ports during a latency time required to stop transmission of the packets in response to said determining as taught by Iliadis in order to avoid losses of in-transit packets (Column 2 Line 37-39).

Regarding to claim 37, Bloch teaches Bloch teaches a system for buffering packets transmitted by a link partner linked to an Infiniband port, comprising: a first memory, for buffering the packets from the port [0009]; flow control logic, configured to advertise to the link partner more buffering resources than are available in said first memory for buffering the packets if space is available in said first memory to buffer the packets, and to advertise no buffering resources if no space is available [0009]; and a second memory, coupled between the port and said first memory, for buffering the packets when no buffering resources are available in said first memory [0043]. Bloch, however, does not explicitly teach a size of said second memory is approximately an amount of data capable of being transmitted to the port during a latency time from when no buffering resources are available in said first memory to when the link partner stops transmitting the packets. Iliadis teaches a size of said second memory is approximately an amount

of data capable of being transmitted to the port during a latency time from when no buffering resources are available in said first memory to when the link partner stops transmitting the packets (Column 4 Line 60). It would have been obvious to one skilled in the art to modify Bloch to have a size of said second memory is approximately an amount of data capable of being transmitted to the port during a latency time from when no buffering resources are available in said first memory to when the link partner stops transmitting the packets as taught by Iliadis in order to avoid losses of in-transit packets (Column 2 Line 37-39).

Regarding to claim 43, Bloch teaches Bloch teaches a system for buffering packets transmitted by a link partner linked to an Infiniband port, comprising: a memory, for buffering the packets from the port [0009]; a buffer controller, for monitoring an amount of free space in said memory [0009]; and flow control logic, configured to advertise to the link partner more buffering resources than are available in said memory for buffering the packets from the port if said buffer controller indicates said amount of free space is above a predetermined threshold [0009], [0053]. Bloch, however, does not explicitly teach said predetermined threshold is approximately an amount of data capable of being transmitted to the port during a latency time from when said buffer controller indicates said amount of free space is below said predetermined threshold to when the link partner stops

transmitting the packets. Iliadis teaches said predetermined threshold is approximately an amount of data capable of being transmitted to the port during a latency time from when said buffer controller indicates said amount of free space is below said predetermined threshold to when the link partner stops transmitting the packets (Column 4 Line 60). It would have been obvious to one skilled in the art to modify Bloch to have said predetermined threshold is approximately an amount of data capable of being transmitted to the port during a latency time from when said buffer controller indicates said amount of free space is below said predetermined threshold to when the link partner stops transmitting the packets as taught by Iliadis in order to avoid losses of in-transit packets (Column 2 Line 37-39).

Regarding to claim 45, Bloch teaches a system for buffering packets transmitted by a link partner linked to an Infiniband port, comprising: a memory, for buffering the packets from the port [0009]; a buffer controller, for monitoring an amount of free space in said memory [0009]; and flow control logic, configured to advertise to the link partner more buffering resources than are available in said memory for buffering the packets from the port if said buffer controller indicates said amount of free space is above a predetermined threshold [0009], [0053], wherein said flow control logic configured to advertise to the link partner said

buffering resources for a plurality of virtual lanes configured on the port (Figure 1), wherein said memory has a size. Bloch, however, does not explicitly teaches the number of said plurality of virtual lanes configured on the port multiplied by a size of at least two maximum-sized Infiniband data packets exceeds said size of said memory. Iliadis teaches the number of said plurality of virtual lanes configured on the port multiplied by a size of at least two maximum-sized Infiniband data packets exceeds said size of said memory (Column 4 Line 54-60). It would have been obvious to one skilled in the art to modify Bloch to have the number of said plurality of virtual lanes configured on the port multiplied by a size of at least two maximum-sized Infiniband data packets exceeds said size of said memory as taught by Iliadis in order to avoid losses of in-transit packets (Column 2 Line 37-39).

3. Claim 15, 17 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bloch et al..

Regarding to claim 15, Bloch teaches a method for buffering packets transmitted to an Infiniband port by an Infiniband device linked to the port, comprising: providing a portion of a memory for buffering the packets, wherein the portion has a size A (See actual spare buffer space in [0009]); transmitting flow control credits to advertise to the device buffering resources of a size B (See

maximum spare allocations in [0009]), wherein B is greater than A; determining when the portion is filled with a predetermined amount of the packets [0053]; and transmitting flow control credits to the device to stop transmission of the packets in response to said determining [0053]; and providing a second memory for buffering the packets transmitted subsequent to said determining [0043], wherein said providing a second memory comprises providing a second memory having a size C [0043]. Bloch, however, does not explicitly teach said size C is between approximately one Kilobyte and approximately sixteen Kilobytes. The actual size of the second memory depends on the size of the packet which the memory is to buffer. It would have been obvious to one skilled in the art to modify Bloch to have a second memory with specific size in order to accommodate to particular specific size of packet.

Regarding to claim 17, Bloch teaches a method for buffering packets transmitted to an Infiniband port by an Infiniband device linked to the port, comprising: providing a portion of a memory for buffering the packets, wherein the portion has a size A (See actual spare buffer space in [0009]); transmitting flow control credits to advertise to the device buffering resources of a size B (See maximum spare allocations in [0009]), wherein B is greater than A; determining when the portion is filled with a predetermined amount of the packets [0053]; and

transmitting flow control credits to the device to stop transmission of the packets in response to said determining [0053]; and buffering the packets transmitted by the device subsequent to said determining in a reserved amount of the portion of the memory, wherein said reserved amount is beyond the predetermined amount [0043]. Bloch, however, does not explicitly teach said size C is between approximately eight Kilobyte and approximately sixteen Kilobytes. The actual size of the second memory depends on the size of the packet which the memory is to buffer. It would have been obvious to one skilled in the art to modify Bloch to have a second memory with specific size in order to accommodate to particular specific size of packet.

Regarding to claim 24, Bloch teaches a method for buffering packets transmitted to an Infiniband port by an Infiniband device linked to the port, comprising: providing a portion of a memory for buffering the packets, wherein the portion has a size A (See actual spare buffer space in [0009]); transmitting flow control credits to advertise to the device buffering resources of a size B (See maximum spare allocations in [0009]), wherein B is greater than A; determining when the portion is filled with a predetermined amount of the packets [0053]; and transmitting flow control credits to the device to stop transmission of the packets in response to said determining [0053], wherein said determining the portion of the

memory is filled a predetermined amount comprises determining an amount of free space in the portion of the memory drops below the predetermined amount [0053]. Bloch, however, does not explicitly teach said amount of free space is between approximately eight Kilobytes and approximately sixteen Kilobytes. The actual size of the free space depends on the size of the packet which the memory is to buffer. It would have been obvious to one skilled in the art to modify Bloch to have a free space with specific size in order to accommodate to particular specific size of packet.

Response to Arguments

4. Applicant's arguments with respect to claim 9-15, 17-22, 24, 26, 28-30, 33, 37, 43 and 45 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clemence Han whose telephone number is (571) 272-3158. The examiner can normally be reached on Monday-Thursday 7 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571) 272-3155. The fax phone

number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C. H.

Clemence Han
Examiner
Art Unit 2665

STEVEN NGUYEN
PRIMARY EXAMINER